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1 Modulo scheduling: Modulo scheduling with integrated register spilling for clustered VLIW architectures
Javier Zalamea, Josep Llosa, Eduard Ayguadé, Mateo Valero
December 2001 **Proceedings of the 34th annual ACM/IEEE international symposium on Microarchitecture**
Publisher: IEEE Computer Society
Full text available: pdf(1.09 MB) Additional Information: full citation, abstract, references, citings
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Clustering is a technique to decentralize the design of future wide issue VLIW cores and enable them to meet the technology constraints in terms of cycle time, area and power dissipation. In a clustered design, registers and functional units are grouped in clusters so that new instructions are needed to move data between them. New aggressive instruction scheduling techniques are required to minimize the negative effect of resource clustering and delays in moving data around.In this paper we pres ...

2 Two-level hierarchical register file organization for VLIW processors
Javier Zalamea, Josep Llosa, Eduard Ayguadé, Mateo Valero
December 2000 **Proceedings of the 33rd annual ACM/IEEE international symposium on Microarchitecture**
Publisher: ACM Press
Full text available: pdf(154.90 KB) ps(843.85 KB) Additional Information: full citation, references, citings, index terms
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3 Compilation: Cluster assignment of global values for clustered VLIW processors
Andrei Terechko, Erwan Le Thénaff, Henk Corporaal
October 2003 **Proceedings of the 2003 international conference on Compilers, architecture and synthesis for embedded systems**
Publisher: ACM Press
Full text available: pdf(330.94 KB) Additional Information: full citation, abstract, references, index terms

In this paper high-level language (HLL) variables that are alive in a whole HLL function, across multiple scheduling units, are termed as global values. Due to their long live ranges and, hence, large impact on the schedule, the global values require different compiler optimizations than local values, which span across only one scheduling unit. The

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